AMENDMENTS TO THE CLAIMS

1. (Amended) A packaging process for a semiconductor package, comprising the steps of:

1) preparing a substrate having a first surface and a second surface, wherein at least one chip-mounting area is formed on the first surface;

2) disposing a plurality of conductive elements on the chip-mounting area of the substrate, wherein the conductive elements are electrically connected to the substrate and each formed with a flat end;

3) forming a first encapsulant on the chip-mounting area of the substrate for encapsulating the conductive elements, wherein the first encapsulant has a top surface [coplanarly formed] formed in coplanar alignment with the flat ends of the conductive elements to thereby form a common coplanar surface, and the ends of the conductive elements are exposed to the outside of the first encapsulant;

4) [mounting] preparing at least one semiconductor chip having a plurality of bond pads formed on a surface thereof, and mounting the semiconductor chip on the top surface of the first encapsulant in a manner that the bond pads [face the substrate, wherein the bond pads] are electrically connected to the exposed ends of the conductive elements respectively and with the surface of the semiconductor chip closely attached to the coplanar surface formed by the first encapsulant and conductive elements free of any gap between the semiconductor chip and the coplanar surface;

5) forming a second encapsulant on the first surface of the substrate for encapsulating the chip; and

6) implanting a plurality of solder balls on the second surface of the substrate, wherein the solder balls are electrically connected to the substrate.

AMENDED VERSION OF THE CLAIMS

1. A packaging process for a semiconductor package, comprising the steps of:

1) preparing a substrate having a first surface and a second surface, wherein at least one chip-mounting area is formed on the first surface;

2) disposing a plurality of conductive elements on the chip-mounting area of the substrate, wherein the conductive elements are electrically connected to the substrate and each formed with a flat end;

3) forming a first encapsulant on the chip-mounting area of the substrate for encapsulating the conductive elements, wherein the first encapsulant has a top surface formed in coplanar alignment with the flat ends of the conductive elements to thereby form a common coplanar surface, and the ends of the conductive elements are exposed to the outside of the first encapsulant;

4) preparing at least one semiconductor chip having a plurality of bond pads formed on a surface thereof, and mounting the semiconductor chip on the top surface of the first encapsulant in a manner that the bond pads are electrically connected to the exposed ends of the conductive elements respectively and with the surface of the semiconductor chip closely attached to the coplanar surface formed by the first encapsulant and conductive elements free of any gap between the semiconductor chip and the coplanar surface;

5) forming a second encapsulant on the first surface of the substrate for encapsulating the chip; and

6) implanting a plurality of solder balls on the second surface of the substrate, wherein the solder balls are electrically connected to the substrate.